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epc OHC15L ESPROS Photonic CMOS® Process

Overview, Options & Services

Version 1.2

Foundry Service Overview

For partners with their own design capability, ESPROS Photonics offers foundry services based on our proprietary ESPROS Photonic CMOS® process. We offer support to you in every aspect of the development process from idea to a product ready to sell. Especially when it comes to the delicate integration of the photonic front-end (e.g. Photodiodes, active pixels, CCD structures etc.), the deep technical understanding of the process is mandatory in order to achieve excellent results.

Process Key Features

- 150nm CMOS process
- CCD trench 90nm
- Wafer size 8"
- Backside processing including thinning, backside contact, AR coating, diffractive filter

Project / Mask Options

We offer Multi Project Wafers (MPW). Wafer runs start on a regular basis.

Mask options are:

- MLM4 with 4 layers (2x2); design area 12 x 15mm^2
- Full mask set (36 masks, useable shot size 25 x 32mm^2)

Packaging Services

ESPROS Photonics delivers products in two of the most advanced and cost-effective packaging technologies. Our IC's are available either in a Quad Flat No-Lead (QFN) or Wafer Level Chip Scale Package (WLCSP). Both packages are RoHS compliant and can easily be assembled with standard SMT assembly equipment. The components come in a 7 inch or 13 inch tape on reel package.

Specific Backend/Packaging services include:

- Testing
- Bumping
- Dicing
- Packaging (CSP, QFN, prototyping)
- Die sort
- Tape on reel

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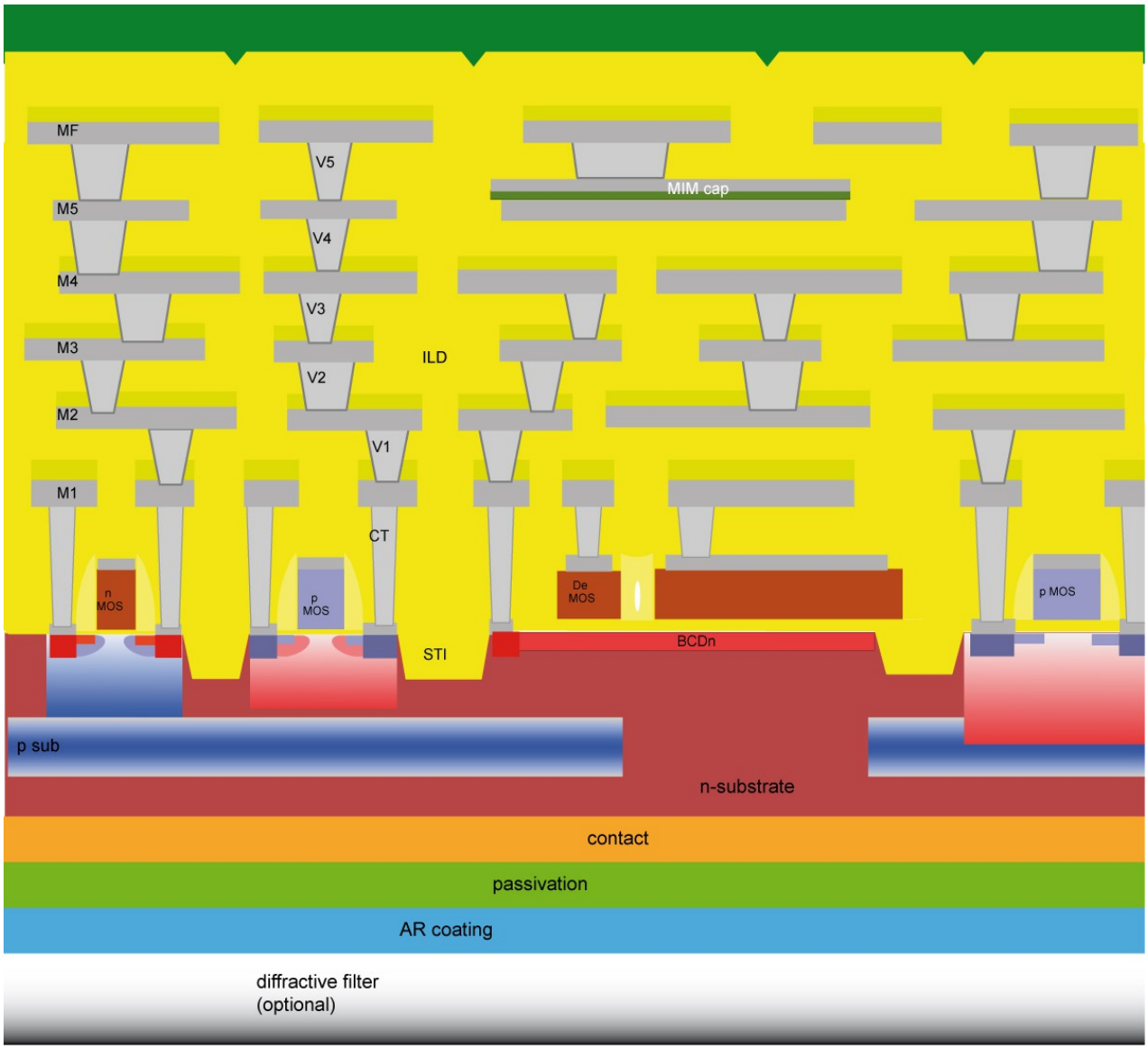
Process Overview

Profile



FrontEnd of Line

- STI
- Implants
- Poly Gates

Mid of Line

- Contact implants
- Salicidation
- Contact formation

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BackEnd of Line

- 6 metal layers
- 5 contact vias
- Final passivation
- Bond pad opening

Backside Processing (optional)

Backside processing is the key to epc's backside illumination (BSI) concept. Wafers are thinned to only 50 micron thickness and anti-reflex coated.

- Contact
- Passivation
- AR coating
- Optional diffractive Filter

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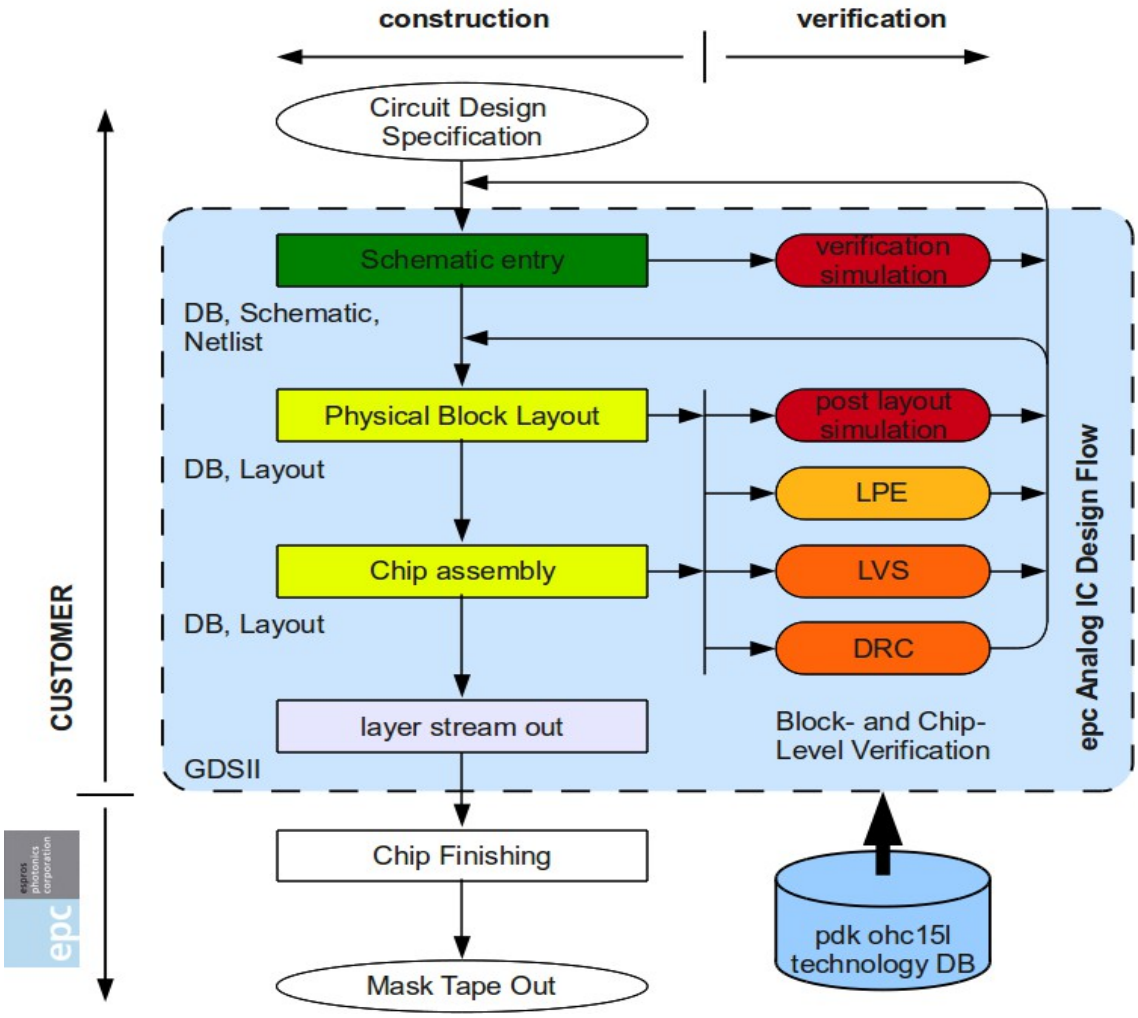
ESPROS Cadence Analog Reference Flow

The ESPROS-Cadence Analog Reference Flow streamlines the process of designing analog/MS chips targeted to our ESPROS Photonic CMOS® process. The flow has been proven through silicon. By taking advantage of ESPROS process technology and Cadence Virtuoso® Custom Design Platform, designers can benefit from a design flow that reduces time-to-silicon and avoids costly re-spins.

Key Benefits:

- productivity
- compatible with Cadence Virtuoso® Custom Design Platform
- predictable path to silicon
- starting point for customized design flow
- reduce development risk

Analog Reference Flow



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ESPROS Photonic CMOS® PDK

ESPROS PDK is a foundry design kit is created to build a bridge between design and foundry. The process design kit includes schematic symbols, techfiles, callback functions for design parameters, parameterized cells for custom layout, schematic-driven layout automation, and provides an easy link to the DRC/LVS/LPE rule deck.ESPROS PDK OHC15L

The following design tools were used in conjunction with the epc Analog IC Design Flow. They represent a subset of the Cadence Custom IC Design platform. The epc OHC15L PDK provides an integrated flow from schematic entry, verification simulation to layout inclusive physical layout verification and postlayout verification simulation.

Task	Candence Tool	Package
Schematic Entry	Virtuoso® Schematic Editor XL	IC610
Simulation Control	Virtuoso® Analog Design Environment	IC610
Verification Simulation	Virtuoso® Spectre® Circuit Simulator	MMSIM101
Post Layout Simulation	Virtuoso® Spectre® Circuit Simulator	MMSIM101
Physical Block Layout	Virtuoso® Layout Editor L, XL, GXL	IC610
Chip assembly	Virtuoso® Layout Editor L, XL, GXL	IC610
Physical Verification		
DRC	Physical Verification System	PVS101
LVS	Physical Verification System	PVS101
LPE	QRC Extraction L	EXT91
Layer stream out	Virtuoso® XStream Out	IC610

Circuit Design

Schematic entry

Virtuoso Schematic Editor is a full-featured, well-proven schematic capture environment capable of supporting analog and mixed-signal integrated circuit designs within the same environment. Through OpenAccess based connected libraries, schematics are seamlessly linked to simulation, layout, verification, and parasitic re-simulation in a continuous, seamless flow.

Circuit Simulation

Analog Design Environment

Designed to help users to create manufacturing-robust designs, Cadence® Virtuoso® Analog Design Environment is the advanced design and simulation environment for the Virtuoso platform. It gives designers access to design verification, new parasitic estimation and comparison flow and optimization algorithms that help to center designs better for yield improvement and advanced matching and sensitivity analyses.

Spectre Circuit Simulator

Cadence® Virtuoso® Spectre® Circuit Simulator provides fast, accurate SPICE-level simulation for tough analog, radio frequency (RF) and mixed-signal circuits. It is tightly integrated with the Virtu-

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oso custom design platform and provides detailed transistor-level analysis in multiple domains. Its superior architecture allows for low memory consumption and high-capacity analysis.

Physical Layout (Block and Chip Level)

Layout

Virtuoso-XL Layout Editor is a full-featured physical block layout editor. Virtuoso XL Layout Editor improves productivity by providing a connectivity and design-rule-driven (DRD) layout editing environment. Virtuoso XL Layout Editor takes advantage of the pCells developed within the ESPROS design kit to rapidly complete circuit block layouts.

Verification

DRC/LVS

Cadence® Physical Verification System (PVS) is the premier Cadence solution for SoC signoff. It integrates with industry-standard digital and custom design flows, enabling designers to procure a front-to-back design and signoff flow from a single EDA vendor. PVS also facilitates a "one tool, one deck" model for digital and custom design that minimizes support overhead.
PVS further offers a unique operation-based distributed processing capability that greatly accelerates throughput without requiring specialized hardware. 100% file compatibility and ease of use make it a drop-in replacement for existing physical verification technologies.

QRC Parasitic Extraction

Cadence QRC Extraction provides best-in-class performance and silicon-proven accuracy for implementation and validation of all complex designs. It is the most comprehensive solution on the market, supporting all nanometer-scale design styles including cell, RF, analog, mixed signal, custom digital, and LCD-TFT. Its advanced capabilities include RLCK extraction, advanced process modeling, multi-corner and statistical extraction, distributed processing, netlist reduction, substrate parasitics extraction, and hierarchical extraction, and it includes an integrated field solver. Integrated with Encounter Digital Implementation System and the Virtuoso custom design platform, Cadence QRC Extraction is the most complete and efficient path to accurate parasitic extraction for all mainstream and advanced node designs.

GDSII Layer Stream Out

The Stream format stores mask generation data for designing integrated circuits. It represents a layout of different design layers the way they finally appear on a chip. The Stream format is widely used in the industry for:

- Archiving design data in interchangeable format.
- Exchanging intellectual property with other vendors.
- Exchanging data between various tools to complete the design cycle.
- Transferring data in a compact form between various design groups.

To translate a design in the Stream format to the OpenAccess database and conversely, you can use the XStream translator. XStream consists of two modules, Stream In and Stream Out. Stream In translates designs in the Stream format to the OpenAccess database. Stream Out translates designs from the OpenAccess database to the Stream format.

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Available Devices for OHC15L Photonic CMOS

All values specified @ 25°C.
(1) Specification values, statistical distribution analysis on large amount of samples is in progress.

MOS

1.8V NMOS - MN

Operation Voltage (OV): Vgs, Vds, Vgb, Vdb, Vsb=1.8V

Absolute Maximum Rating (AMR): Vgs, Vds, Vgb, Vdb, Vsb=2.0V

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
VT_{lin}	W/L 10/0.15µm	V	0.485(1)	0.55	0.615(1)	
VT_{lin}	W/L 10/10µm	V	0.245(1)	0.275	0.305(1)	
VT_{lin}	W/L 0.32/0.15µm	V	0.425(1)	0.500	0.575(1)	
IDS/W	W/L 10/0.15cm	µA/µm	590(1)	670	750(1)	
I_{off}	W/L 10/0.15µm	pA/µm		5	70(1)	
BV_{off}	Ids=1µA	V	4.0(1)	4.3		

1.8V PMOS - MP

Operation Voltage (OV): Vgs, Vds, Vgb, Vdb, Vsb=1.8V

Absolute Maximum Rating (AMR): Vgs, Vds, Vgb, Vdb, Vsb=2.0V

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
VT_{lin}	W/L 10/0.15µm	V	-0.490(1)	-0.550	-0.610(1)	
VT_{lin}	W/L 10/10µm	V	-0.515(1)	-0.550	-0.585(1)	
VT_{lin}	W/L 0.32/0.15µm	V	-0.460(1)	-0.530	-0.600(1)	
IDS/W	W/L 10/0.15µm	µA/µm	-200(1)	-265	-330(1)	
I_{off}	W/L 10/0.15µm	pA/µm		-2	-70(1)	
BV_{off}	Ids=1µA	V	-4.0(1)	-4.3		

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5V NMOS - MN5

Operation Voltage (OV): Vgs, Vds, Vgb, Vdb, Vsb=5.0V

Absolute Maximum Rating (AMR): Vgs, Vds, Vgb, Vdb, Vsb=5.5V

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
VT_{lin}	W/L 10/0.55µm;	V	0.67(1)	0.75	0.82(1)	spec
VT_{lin}	W/L 10/10µm;	V	0.72(1)	0.8	0.88(1)	
VT_{lin}	W/L 0.32/0.55µm;	V	0.5(51)	0.65	0.7(51)	
IDS/W	W/L 10/0.55µm;	µA/µm	480(1)	560	640(1)	
I_{off}/W	W/L 10/0.55µm;	pA/µm		0.35	2(1)	
BV_{off}	Ids=1µA	V	11(1)	12	13	

5V PMOS - MP5

Operation Voltage (OV): Vgs, Vds, Vgb, Vdb, Vsb=5.0V

Absolute Maximum Rating (AMR): Vgs, Vds, Vgb, Vdb, Vsb=5.5V

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
VT_{lin}	W/L 10/0.6µm;	V	-0.7(1)	-0.75	-0.8(1)	
VT_{lin}	W/L 10/10µm;	V	-0.73	-0.78	-0.83	
VT_{lin}	W/L 0.32/0.6µm;	V	-0.62	-0.67	-0.720	
IDS/W	W/L 10/0.6µm;	µA/µm	-235(1)	-275	-310(1)	
I_{off}/W	W/L 10/0.6µm;	pA/µm	-1	-0.6		
BV_{off}	W/L 10/0.6µm; Ids=1µA	V	-9(1)	-10		

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12V NDEMOS - MND12

Fixed Connections: Vsb=0V

Operation Voltage (OV): Vds, Vdb, Vgd=12.0V

Operation Voltage (OV): Vgs, Vgb=5.0V

Absolute Maximum Rating (AMR): Vds, Vdb, Vgd=13.5V

Absolute Maximum Rating (AMR): Vgs, Vgb=5.5V

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
VT_{lin}	W/L 10/1µm;	V	0.75[1]	0.85	0.95[1]	
VT_{lin}	W/L 10/10µm;	V	0.7[1]	0.8	0.9[1]	
VT_{lin}	W/L 0.32/1µm;	V	0.6[1]	0.7	0.8[1]	
IDS/W	W/L 10/1µm;	µA/µm	290[1]	320	350[1]	
I_{off}/W	W/L 10/1µm;	pA/µm		0.5	1[1]	
BV_{off}	W/L 10/1µm; Ids=1µA	V	26[1]	28		

12V PDEMOS - MPD12

Fixed Connections: Vsb=0V

Operation Voltage (OV): Vds, Vdb, Vgd=-12.0V

Operation Voltage (OV): Vgs, Vgb=-5.0V

Absolute Maximum Rating (AMR): Vds, Vdb, Vgd=-13.5V

Absolute Maximum Rating (AMR): Vgs, Vgb=-5.5V

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
VT_{lin}	W/L 10/0.75µm;	V	-0.65[1]	-0.8	-0.95[1]	
VT_{lin}	W/L 10/10µm;	V	-0.65[1]	-0.8	-0.95[1]	
VT_{lin}	W/L 0.32/0.75µm;	V	-0.55[1]	-0.7	-0.85[1]	
IDS/W	W/L 10/0.75 µm;	µA/µm		-200[1]		
I_{off}/W	W/L 10/0.75 µm;	pA/µm	-2	-0.4[1]		
BV_{off}	W/L 10/1µm; Ids=1µA	V		-21[1]		

12V Depletion MN12d

Fixed Connections: Vsb=0V

Operation Voltage (OV): Vds, Vdb, Vsb=12.0V

Operation Voltage (OV): Vgs, Vgd, Vgb <5.0V (channel on)

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Operation Voltage (OV): Vgs, Vgd, Vgb >-12.0V (channel depleted)

Absolute Maximum Rating (AMR): Vds, Vdb, Vsb=13.5V

Absolute Maximum Rating (AMR): Vgs, Vgd, Vgb <5.5V (channel on)

Absolute Maximum Rating (AMR): Vgs, Vgd, Vgb >-13.5V (channel off)

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
VT_{lin}	W/L 10/0.88µm;	V	-1[(1)]	-1.2	-1.4[(1)]	
VT_{lin}	W/L 10/10µm;	V		NA		
VT_{lin}	W/L 0.32/0.88µm;	V	-0.7[(1)]	-0.9	-1.1[(1)]	
IDS/W	W/L 10/0.88µm;	µA/µm		150		
I_{off}/W	W/L 10/1µm;	pA/µm		5	50[(1)]	
BV_{off}	W/L 10/1µm; Ids=1µA	V		30		

Bipolar

5V LPNP - QPNPL5x5

Operation Voltage (OV): V_{BE}, V_{BC}, V_{CB}=-5.0V

Absolute Maximum Rating (AMR): V_{BE}, V_{BC}, V_{CB}=-5.5V

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
BV_{CEO}	@I_{CE}=-1µA	V	-10[(1)]	-11	-12[(1)] [(1)]	
BV_{CES}	@I_{CE}=-1µA	V	-10[(1)]	-11	-12	
h	@V_{CE}=-2V @I_{CE}=-100µA		25[(1)]	35	45[(1)]	
V_{BE}	@I_{CE}=-10µA	V		0.7[(1)]		

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Diodes

NSD/Pwell Diode - DN

Operation Voltage (OV): $V_{reverse}$=-5.0V

Absolute Maximum Rating (AMR): $V_{reverse}$=-7.0V

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
BV	@I=1µA	V	12[1]	13	14[1]	
V_{BE}	@I=10µA	V		0.7		

PSD/Nwell Diode - DP

Min, typ and max are given at 25°C

Operation Voltage (OV): $V_{reverse}$=5.0V

Absolute Maximum Rating (AMR): $V_{reverse}$=7.0V

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
BV	@I=1µA	V	11.6[1]	11.2[1]	10.8[1]	
V_{BE}	@I=10µA	V		0.69		

PSD/HVnwell Diode - DP5

Operation Voltage (OV): $V_{reverse}$=5.0V

Absolute Maximum Rating (AMR): $V_{reverse}$=7.0V

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
BV	@I=1µA	V	13[1]	14[1]	15[1]	
V_{BE}	@I=10µA	V		0.69		

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Resistors

High resistance Poly resistor - RNHR

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
Resistance	L=240µm, W=0.15µm; @I=2µA	Ohm/q		2200		

Not salicided NSD poly resistor - RNNPO

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
Resistance	L=240µm, W=0.15µm; @I=2µA	Ohm/q		170		
Resistance	L=240µm, W=2µm; @I=10µA	Ohm/q		120		

Not salicided PSD poly resistor – RNPO

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
Resistance	L=240µm, W=0.15µm; @I=2µA	Ohm/q		400		

Metal resistor

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
MET1-5 Resistance	L=240µm, W=0.24µm; @I=1mA	Ohm/q		0.08		
MET1-5 Resistance	L=240µm, W=2µm; @I=4mA	Ohm/q		0.011		
MET1-5 Resistance	L=240µm, W=0.24 µm; @I=10mA	Ohm/q		0.04		
MET1-5 Resistance	L=240µm, W=2 µm; @I=10mA	Ohm/q		0.04		

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Contact and Vias resistance

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
Contact over N+ Active		Ohm		10 (1)		
Contact over P+ Active		Ohm		10 (1)		
Contact over Poly		Ohm		10 (1)		
Via 1-4		Ohm		3.5(1)		
ViaMIM		Ohm		5.5(1)		
Tvia		Ohm		3.7(1)		

Capacitors

MIM cap

Parameter	Conditions	Units	Specifications			Notes
			min	typ	max	
Capacitance		$fF/\mu m^2$		0.98		

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Available IP

A variety of IP blocks has been developed and can be accessed for product development with our PDK.

- Photo diodes incl. Pcells
- Buried channel CCD incl. Pcells
- 3D-TOF pixel
- Amplifiers (TIA, Video, LNA)
- Filters
- Bandgap
- Voltage references, voltage regulators and current sources
- Charge pumps (up and down)
- Various oscillators
- PLL
- DLL
- ADC
- DAC
- Temperature sensors
- Various digital-logic blocks
- Input and output devices
- 2-wire inter-chip communication
- EEPROM cells and blocks

ESPROS Photonics "IP-Store" Program

ESPROS IP Store offers you the possibility to make your IP developments commercially available. Generate additional turnover by licensing your IP blocks as library elements in our PDK. Participation in the ESPROS Photonics IP-Store Program is based on customer-individual contracts.

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